

Indeed, this rejection has been rendered moot by incorporating the limitations of claim 2 therein, claim 2 not being subject to this rejection. Accordingly, the Examiner has implicitly acknowledged that present claim 1 is not identically described by Hashimoto et al. Applicant, therefore, submits that the imposed rejections of claims 1, 3 and 4 under 35 U.S.C. §102 for lack of novelty as evidenced by Hashimoto et al. is not factually viable and, hence, solicits withdrawal thereof.

**Claims 2 and 6 were rejected under 35 U.S.C. §103 for obviousness predicated upon Hashimoto et al. in view of Ando et al.**

In the statement of the rejection, the Examiner admitted that Hashimoto et al. do not disclose the invention defined in claim 2 (now claim 1), notably a semiconductor device wherein the recited SRAM comprises an access MOS transistor and a driver MOS transistor. This rejection is traversed.

Initially, Applicant will treat this rejection as though applied against claim 1, since the limitations of claim 2 have been incorporated into claim 1, and claim 2 cancelled. Applicant submits that the applied references, taken singly or in combination, do not disclose or suggest the structure now defined in independent claim 1. Ergo, even **if** the applied references are combined, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 USPQ2d 1434 (Fed. Cir. 1988).

Specifically, although Ando et al. may disclose an SRAM, Ando et al. neither disclose nor suggest that the surface of the active region of the access MOS transistor is entirely rounded. Similarly, Hashimoto et al., do not disclose that the surface of the active region of the access

MOS transistor is entirely rounded. Indeed, Hashimoto et al. neither disclose nor suggest that the surface of the active region of the transistors in a memory cell is rounded.

The above argued **differences** between the claimed invention and **each** of the applied references compel the conclusion that even **if** the applied references are combined, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., supra*. Applicant, therefore, submits that the imposed rejection of claim 2 (now claim 1) and claim 6 under 35 U.S.C. §103 for obviousness predicated upon Hashimoto et al. in view of Ando et al. is not factually or legally viable and, hence, solicits withdrawal thereof.

**Claim 5 was rejected under 3 U.S.C. §103 for obviousness predicated upon Hashimoto et al. in view of Ando et al. and Kuriyama et al.**

This rejection is traversed. Specifically, claim 5 depends from independent claim 1. Applicant incorporates herein the arguments previously advanced in traversing the imposed rejection of claim 2 (now claim 1) under 35 U.S.C. §103 for obviousness predicated upon Hashimoto et al. in view of Ando et al. The additional reference to Kurayima et al. does not cure the argued deficiencies in the attempted combination of Hashimoto et al. and Ando et al. Ergo, even **if** the applied references are combined, the claimed invention would **not** result. *Uniroyal, Inc. v. Rudkin-Wiley Corp., supra*.

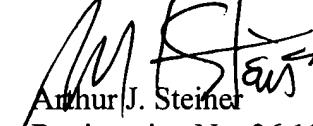
Applicant, therefore, submits that the imposed rejection of claim 5 under 35 U.S.C. §103 for obviousness predicated upon Hashimoto et al. in view of Ando et al. and Kuriyama et al. is not factually or legally viable and, hence, solicits withdrawal thereof.

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Accordingly, favorable consideration is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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## APPENDIX

Claim 1 now reads as follows.

1. (Amended) A semiconductor device, comprising:
- a semiconductor substrate including an active region and an isolation region; and
- a gate electrode formed on said active region with an insulating film interposed therebetween, wherein:
- a surface of said active region is entirely rounded so as to be inclined downward toward said isolation region;
- said semiconductor device includes an SRAM (Static Random Access Memory);
- said SRAM includes an access MOS (Metal Oxide Semiconductor) transistor and a drive MOS transistor; and
- the surface of said active region of said access MOS transistor is entirely rounded.

Claim 2 has been cancelled.